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APPLICATION FOR LETTERS PATENT

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Capacitors and Methods Of Forming Capacitors

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CAPACITORS AND METHODS OF FORMING CAPACITORS

TECHNICAL FIELD

This invention relates to capacitors and to methods of forming capacitors.

BACKGROUND OF THE INVENTION

Typical capacitors comprise a pair of conductive electrodes spaced apart by intervening capacitor dielectric material. As integrated circuitry becomes denser and as individual electronic components such as capacitors get smaller, integrated circuitry fabricators face the challenge of developing capacitor constructions and materials which achieve desired capacitance despite the decreasing size. Example materials under consideration for capacitor dielectric layers include titanates and tantalum pentoxide. These and other capacitor dielectric layer materials can occur in crystalline and in amorphous phases.

It is generally known that the capacitance of dielectric materials such as these can, at least initially, be increased from their as-deposited form by annealing. Such annealing can promote crystallization, re-crystallization or crystal realignment which can facilitate increase in capacitance and reduction in current leakage through the material. However, such annealing can also cause single crystals to be formed in the dielectric layer which in essence extend entirely through the

dielectric layer between the layer's opposing surfaces. Annealing or crystal formation to this degree can undesirably have the effect of increasing current leakage. This is primarily due to continuous paths being provided by the continuous grain boundaries for current leakage from one side of the layer to the other. It would be desirable to improve upon these adverse characteristics of capacitor dielectric layer materials.

SUMMARY OF THE INVENTION

The invention in one aspect includes methods of forming capacitors and to capacitor constructions. In one implementation, a method of forming a capacitor includes forming a first capacitor electrode. A first layer of a first capacitor dielectric material is formed over the first capacitor electrode. A second layer of the first capacitor dielectric material is formed on the first layer. A second capacitor electrode is formed over the second layer of the first capacitor dielectric material. In accordance with another implementation, the first layer comprises a first titanate compound comprising capacitor dielectric material and the second layer comprises a different second titanate compound comprising capacitor dielectric material. A capacitor in accordance with an implementation of the invention includes a pair of capacitor electrodes having capacitor dielectric material therebetween comprising a composite of two immediately juxtaposed and contacting, yet discrete, layers of the same capacitor dielectric material. A

capacitor in accordance with another implementation includes a pair of capacitor electrodes having capacitor dielectric material therebetween comprising a composite of two immediately juxtaposed and contacting, yet discrete, layers of two different capacitor dielectric materials, said two capacitor dielectric materials including two different titanate compounds. A capacitor in accordance with still another implementation includes a pair of capacitor electrodes having capacitor dielectric material therebetween comprising a composite of two immediately juxtaposed and contacting, yet discrete, layers of two different capacitor dielectric materials, one of the two different materials comprising a titanate compound and the other comprising Ta_2O_5.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a wafer fragment at one processing step in accordance with the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 4.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

A semiconductor wafer in process in accordance with one aspect of the invention is indicated in Fig. 1 with reference numeral 10. Such comprises a semiconductive substrate in the form of a bulk monocrystalline silicon substrate 12. In the context of this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. A first capacitor electrode 16 is formed over substrate 12. Exemplary materials include conductively doped polysilicon or TiN. An exemplary thickness for layer 16 is from 100 Angstroms to 1500 Angstroms.

A first layer 18 of a first capacitor dielectric material is formed over first capacitor electrode 16. Exemplary and preferred materials

include barium strontium titanate (BST), strontium titanate (ST), strontium bismuth titanate (SBT), lead lanthanate zirconia titanate (PLTZ), Ta_2O_5, and mixtures thereof. The preferred method of depositing layer 18 is by chemical vapor deposition. Layer 18 as initially formed can be either crystalline or amorphous, with an initial amorphous structure being preferred and shown in the fabrication of a capacitor dielectric layer in accordance with this aspect of the invention. Regardless, first layer 18 of first capacitor dielectric material is preferably subsequently annealed at a temperature of at least 300°C for a time period sufficient to achieve a selected crystalline structure intended to densify and facilitate capacitive properties of such material (Fig. 2). Exemplary anneal conditions include a temperature range of from about 300°C to about 1200°C at a pressure of from about 2 mTorr to about 5 atm for a treatment time of anywhere from about 1 minute to 2 hours. Unfortunately as described above with respect to the prior art, such annealing can cause sufficient recrystallization to form singular grains at various locations throughout layer 18 having grain boundaries which extend from one surface of the layer to the other, as shown.

Referring to Fig. 3, a second layer 20 of the same first capacitor dielectric material of layer 18 is formed on first layer 18 after the preferred layer 18 annealing. Second layer 20 is also preferably chemical vapor deposited, and can initially be formed to be amorphous or crystalline. Preferably, it is initially formed to be amorphous as

shown. Further, the thickness of first layer 18 of the first material is preferably chosen to be from about 10% to about 90% of the finished combined thickness of first layer 18 and second layer 20. An exemplary thickness range for the combination of layers 18 and 20 is from 60 Angstroms to 1000 Angstroms. By way of example only where the material of layers 18 and 20 comprises BST, an example thickness for each layer 18 and 20 is 150 Angstroms.

Referring to Fig. 4, a second capacitor electrode 22 is formed over second layer 20 of the first capacitor dielectric material. An exemplary thickness range for electrode 22 is from 100 Angstroms to 2500 Angstroms. Further, diffusion barrier layers, if desired, can be positioned anywhere intermediate the composite of layers 18 and 20, and first electrode 16 and second electrode 22. Regardless, it is most preferable that second layer 20 of the first material not be exposed to a temperature of 500°C or greater before deposition of any subsequent layer thereover. In certain instances, exposure to such temperature for a sufficient period of time could cause complete crystal realignment relative to the composite layer of layers 18 and 20, and undesirably form grain boundaries which extend from the base of layer 18 clear through to the top of layer 20.

Electrode layer 22 and/or any intervening diffusion barrier or other layer provided over layer 20 are chosen and deposited in such a way that a degree of desired stress (either tensile or compressive) will be imparted into layer 20, either during formation/deposition or subsequently

such as when it is heated. Such stress can be imparted inherently by the electrode material during its deposition, or by choosing deposition/forming conditions that themselves impart a desired stress. For example, selection of temperature and pressure conditions during deposition/formation of the electrode layer can be selected to impart a desired stress regardless of the electrode material being deposited. Alternately, the material can be chosen relative to the second capacitor dielectric layer to impart a desired tensile or compressive stress. Such example materials for use with the preferred titanates and pentoxides capacitor dielectric layers include TiN_X, WN_X, TaN_X, $PtRh_X$, $PtRu_X$, $PtIr_X$, and mixtures thereof. Further alternately, and by way of example only, the second capacitor electrode material could be doped with a conductivity enhancing impurity during its formation chosen to achieve a selected stress on the second layer of the capacitor dielectric layer.

Regardless, such stress can largely prevent complete recrystallization of the same material of layers 18 and 20. Exemplary dedicated anneal conditions include temperatures ranging from 500°C to 1000°C, and pressures ranging from 50 mTorr to 50 atmospheres. Accordingly, layer 20 is preferably ultimately annealed either with a dedicated anneal step or in conjunction with other wafer processing to render it substantially crystalline in its finished composition. Regardless, the preferred capacitor construction will comprise a pair of capacitor electrodes having capacitor dielectric material therebetween comprising

a composite of two immediately juxtaposed and contacting, yet discrete, layers of the same capacitor dielectric material, as shown.

Accordingly in the above-described preferred embodiment, first layer 18 of the capacitor dielectric layer material is essentially provided with a selected finished crystalline structure prior to formation of second layer 20 thereon. Such is achieved by the crystallization or recrystallization anneal immediately prior to formation of layer 20. Also in the preferred embodiment, the final composition of second layer 20 of the first material is also desirably formed to be crystalline, although alternately such could remain amorphous if so initially deposited. In the preferred embodiment for a capacitor dielectric layer where both of layers 18 and 20 are crystalline in their final form, an interface line 19 essentially forms therebetween where such discrete layers contact (Fig. 5). Interface line 19 is characterized by a perceptible change in crystallinity from one layer to the other, such as shown or evidenced in this example by a substantial lateral shift or displacement in grain boundaries from one layer to the other.

In accordance with another implementation of the invention, first layer 18 can comprise a first titanate compound and second layer 20 can comprise a different second titanate compound. In accordance with still another implementation of the invention, first layer 18 can comprise one capacitor dielectric layer material and second layer 20 can comprise another different capacitor dielectric layer material, with one of the materials comprising a titanate compound and the other comprising

Ta_2O_5. By way of example only, example titanate compounds are those referred to above.

Fluorine or other grain boundary passivation treatments can also be conducted relative to the first and second layers of material intermediate or after such layers have been deposited. Example such treatments are described in our U.S. Patent No. 5,665,611 and references cited therein.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.